WE CLAIM:

1. A magneto-resistive cell in a magneto-resistive random access memory (MRAM), comprising:

a first magneto-resistive bit with a first terminal and a second terminal, where the first terminal is coupled to a first word line;

a second magneto-resistive bit with a first terminal and a second terminal, where the first terminal is coupled to a second word line;

a first switch with a gate, a source, and a drain, where the drain is coupled to the second terminal of the first magneto-resistive bit, and where the source is coupled to a voltage reference; and

a second switch with a gate, a source, and a drain, where the drain is coupled to the second terminal of the second magneto-resistive bit, and where the source is coupled to the voltage reference, and where the gate of the second switch is coupled to the gate of the first switch and to a select line.

2. The magneto-resistive cell as defined in Claim 1, wherein the first switch and the second switch are configured to provide at least two resistive modes at least partially in response to a state of the select line, where an intermediate resistance mode limits an amount of current drawn from the first word line and the second word line during a write operation, and where a lower resistive mode decreases an amount of resistance in series with the first magneto-resistive bit and in series with the second magneto-resistive bit during a read operation.

3. The magneto-resistive cell as defined in Claim 2, wherein the first switch and the second switch are further configured to provide at least a third mode at least partially in response to a state of the select line, where the third mode corresponds to a higher resistive mode that substantially prevents current from the first word line and the second word line from flowing through the first magneto-resistive bit and the second magneto-resistive bit via the first switch or the second switch.

4. The magneto-resistive cell as defined in Claim 1, wherein the first switch and the second switch correspond to metal oxide semiconductor field effect transistors (MOSFETs).

5. The magneto-resistive cell as defined in Claim 1, wherein the voltage reference is ground.

6. The magneto-resistive cell as defined in Claim 1, wherein a state of the select line is responsive to a memory address.

7. The magneto-resistive cell as defined in Claim 1, further comprising a third switch with a gate, a source, and a drain, where the gate is coupled to a write line for control,

where the drain is coupled to the first word line, and where the source is coupled to the second word line, where in a first state, the third switch electrically isolates the first word line and the second word line, and in a second state, the third switch is conductive so that at least a portion of the word current on the first word line is provided to the second word line.

8. The magneto-resistive cell as defined in Claim 7, wherein the first state corresponds to a read mode and the second state corresponds to a write mode.

9. A memory array in a magneto-resistive random access memory (MRAM), comprising:

a plurality of magneto-resistive cells, where a magneto-resistive cell from the plurality has a first magneto-resistive bit, a second magneto-resistive bit, a first switch, and a second switch so that there are a plurality of first magneto-resistive bits, a plurality of second magneto-resistive bits, a plurality of first switches, and a plurality of second switches, where a first magneto-resistive bit has a first terminal and a second terminal, where a second magneto-resistive bit has a first terminal and a second terminal;

where the plurality of magneto-resistive cells are arranged so that first terminals of the plurality of first magneto-resistive bits are coupled to a first word line and first terminals of the plurality of second magneto-resistive bits are coupled to a second word line;

where the plurality of magneto-resistive cells are arranged so that drains of the plurality of first switches are coupled to first terminals of respective first magneto-resistive bits;

where the plurality of magneto-resistive cells are arranged so that drains of the plurality of second switches are coupled to first terminals of respective second magneto-resistive bits;

where the plurality of magneto-resistive cells are arranged so that sources of the plurality of first switches and the plurality of second switches are coupled to a voltage reference; and

where the plurality of magneto-resistive cells are arranged so that gates of a first switch and a second switch for a magneto-resistive cell are coupled together and coupled to a control.

10. The memory array as defined in Claim 9, further comprising additional pluralities of magneto-resistive cells.

11. The memory array as defined in Claim 9, wherein the first switch and the second switch for a magneto-resistive cell are configured to provide at least two resistive modes at least

partially in response to a state of a control provided as an input to the gates of the first switch and the second switch, where an intermediate resistance mode limits an amount of write sense current drawn from the first word line or the second word line during a write operation, and where a lower resistive mode decreases an amount of resistance in series with the first magneto-resistive bit and the second magneto-resistive bit during a read operation.

12. The memory array as defined in Claim 11, wherein the first switch and the second switch are further configured to provide at least a third mode at least partially in response to a state of the control, where the third mode corresponds to a higher resistive mode that substantially prevents current from the word line from flowing through the first magneto-resistive bit and the second magneto-resistive bit via the first switch or the second switch.

13. The memory array as defined in Claim 9, wherein the first switch and the second switch correspond to metal oxide semiconductor field effect transistors (MOSFETs).

14. The memory array as defined in Claim 9, wherein the voltage reference is ground.

15. The memory array as defined in Claim 9, wherein the control is at least partially responsive to a memory address.

16. The memory array as defined in Claim 9, further comprising a third switch with a gate, a source, and a drain, where the gate is coupled to a write line for control, where the drain is coupled to the first word line, and where the source is coupled to the second word line, where in a first state, the third switch electrically isolates the first word line and the second word line, and in a second state, the third switch is conductive so that at least a portion of the word current on the first word line is provided to the second word line.

17. The memory array as defined in Claim 16, wherein the first state corresponds to a read mode and the second state corresponds to a write mode.

18. A magneto-resistive cell for a magneto-resistive random access memory (MRAM), comprising:

an electrically-conductive line coupled to a first source of current for a write current and to a second source of current for a read current;

a magneto-resistive memory bit with a first terminal and a second terminal, where a first terminal is coupled to the electrically-conductive line and is adapted to receive current carried by the electrically-conductive line for both the write current and the read current; and

a controllable resistance coupled to the second terminal of the magneto-resistive bit and to a voltage reference.

19. The magneto-resistive cell as defined in Claim 18, wherein the controllable resistance is configured to provide at least two resistive modes, where an intermediate resistance mode limits an amount of current drawn during a write operation, and where a lower resistive mode decreases an amount of resistance in series with the magneto-resistive memory bit during a read operation.

20. The magneto-resistive cell as defined in Claim 19, wherein the controllable resistance is further configured to provide at least a third mode, where the third mode corresponds to a higher resistive mode that substantially prevents current from flowing through the magneto-resistive memory bit via the controllable resistance.

21. The magneto-resistive cell as defined in Claim 18, wherein the voltage reference corresponds to ground.